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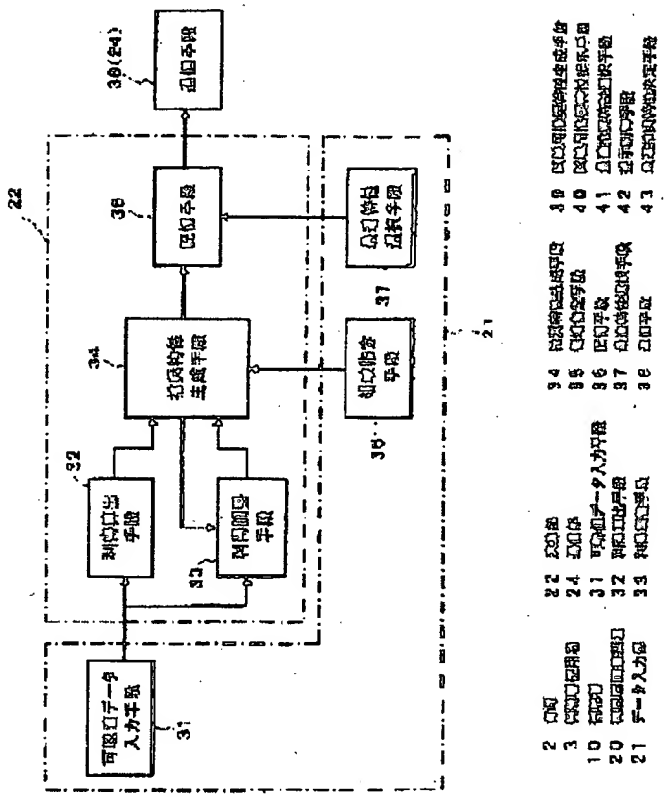
TITLE : HEARING AID ADJUSTMENT DEVICE AND THE HEARING AID



ABSTRACT : PROBLEM TO BE SOLVED: To provide a hearing aid adjustment device and the hearing aid by which recommended characteristics of a hearing aid matching the user can be obtained without relying on the skill of a salesman resulting in stabilized adjustment accuracy.

SOLUTION: The hearing aid adjustment device is provided with an audible value data entry means 31 that enters a minimum audible value and an uncomfortable threshold relating to one sound source 2 of a hearing aid user 3, a gain calculation means 32 that calculates the gain for each frequency within an audible frequency band from the minimum audible value up to the unpleasant threshold entered by the audible value data entry means 31, a gain adjustment means 33 that selects a frequency within the audible frequency band and adjusts the gain of the selected frequency, and a recommended characteristic generating means 34 that generates a recommended characteristic of a hearing aid 10 on the basis of the gain at the frequency adjusted by the gain adjustment means 33 and the gains of frequencies other than the frequency whose gain is adjusted.

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PATENT SPECIFICATION

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(19)

(54) INPUT SIGNAL LEVEL CONTROL FOR COMMUNICATIONS CHANNELS

(71) We, NATIONAL RESEARCH DEVELOPMENT CORPORATION, a British Corporation established by Statute, of Kingsgate House, 66—74 Victoria Street, London, S.W.1, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to the adjustment of the level of electrical signals in communication channels, and particularly but not exclusively to the level adjustment of signals representing speech in the transmitters of two-way radio systems. "Level" is used in a general sense and is intended to mean any characteristic of the signal which depends on the instantaneous magnitudes of the signal.

Automatic level control may be used with advantage at the input of virtually any speech transmission or recording system. If the input signal can be held at a constant and maximum value, then the best transmission signal to noise ratio is obtained. Distortion due to overload is also avoided.

According to a first aspect of the present invention there is provided apparatus for automatic signal level adjustment, including processing means for measuring the value of a characteristic of each of successive portions of an input signal, the portions being consecutive or separated by intervals, and the characteristic of each portion being related to the magnitude of at least one instantaneous value of the signal in that portion and the processing means also being arranged to operate on each portion of the input signal, in accordance with the value measured for that portion only provided the measured value is above a predetermined limiting threshold value, to provide an output signal having successive portions in each of which the same characteristic, or another characteristic related to the magnitude of at least one instantaneous value in that portion, is brought within a predetermined range of values.

The apparatus will be recognised as applying feedforward control.

Assuming a cyclic input signal, each said portion is preferably less than ten half cycles of the input signal in duration.

The characteristic of a portion may for example be the median magnitude of the instantaneous values, or the mean or r.m.s. of these values. Preferably, however, the characteristic is the peak magnitude (that is the amplitude) occurring in the portion although any root, that is square root, cube root and so on, of the peak magnitude may be used. The controlled characteristic of the output signal is preferably also the peak magnitude occurring in the portion and again it is preferable that the operation carried out by the processing means is one of bringing all peak magnitudes, except those corresponding to input signal peaks below the predetermined threshold value, to substantially the same magnitude; that is the predetermined range is reduced as nearly as practically possible to a single value.

In addition to its dependence on the magnitude of one or more instantaneous values the characteristic may depend on the polarity of the value or values.

The operation carried out by the processing means on the input signal is preferably one of amplification or attenuation determined by a control signal which is linearly or non-linearly related to the measured values of the characteristic.

The successive portions are preferably consecutive and the duration of each said portion of the input signal is preferably half a cycle. The control signal is then varied, when necessary, at the beginning of each half cycle. In this specification the term "half cycle" means that portion of a signal having one polarity which occurs between successive portions having the opposite polarity, and the term is not intended to imply that two successive half cycles, one

of one polarity and the other of the other polarity, are similar in wave shape or in any other way.

The processing means preferably compares each value of the measured characteristic with a reference signal corresponding to the above-mentioned threshold value, and varies the amplification carried out from a constant value or unity to a variable value only if the measured value of a characteristic is greater than the reference signal.

With the peak magnitude of each half cycle controlling the amplication of that half cycle and bringing all peaks above the threshold value to the same magnitude, the following advantages are obtained:

(a) Tight control of the peak amplitude of the speech waveform. The shape of each half cycle of waveform remains substantially unaltered, although all peaks are of equal amplitude.

(b) A rapid response. The output level is at all times defined by the control signal but there is an inescapable delay which is equal to the longest interval between zero crossings in the expected waveform.

(c) Low distortion. The distortion depends on the change in slope of the waveform as it passes through zero and is greater for waveforms having a successive peaks of widely varying magnitudes.

(d) A decrease in the peak-to-r.m.s. ratio of the waveform. By bringing up the smaller peaks to the level of the largest, the r.m.s. level is increased without increasing the overall amplitude.

(e) Relatively simple implementation. The peaks of the waveforms are easily measured whereas measurement of the average of r.m.s. level of each half cycle would require the division of the time between zero crossings.

Other advantages are discussed below with reference to Figures 6, 7 and 8. As is mentioned below apparatus with a working frequency range of 50 Hz to 6 KHz may be constructed.

If the characteristic is measured over two or more intervals between zero crossings and the gain is adjusted at the beginning of each such group of intervals, then the speech waveform will retain its pattern for a longer period and there is a possibility of improvement in speech quality.

Alternatively, processing means may measure the characteristic over a pitch period for voiced sounds, and over a fixed interval, for example eight to ten zero crossings, for unvoiced sounds; the processing means measuring the pitch period and switching to the fixed interval during unvoiced sounds.

The said predetermined threshold value may be regarded as a limiting threshold below which signals are amplified by a constant factor. In some circumstances it is useful to have a zero threshold when the said predetermined threshold value is zero.

Instead of using a single limiting threshold several thresholds may be employed and the gain applied varied according to the relationship between the measured characteristic and the various thresholds.

If the lower threshold is regarded as a noise threshold, the gain below the noise threshold may be unity or some other low value above or below unity, and consequently noise during intervals between speech is not accentuated.

Additionally means may be provided for measuring the signal to noise ratio and varying the noise threshold or thresholds in dependence upon the measured ratio. Alternatively the processing means may vary the limiting threshold according to speech level measured over a predetermined interval. Similarly the processing means may vary the noise threshold according to measured noise level measured in intervals when speech is absent.

The processing means may include a programmed microprocessor and an associated memory, although some, or all, functions may be performed by special purpose circuits.

Where apparatus according to the first aspect of the invention includes a microprocessor, the apparatus may also include a sample-and-hold circuit for sampling analogue signals and an analogue-to-digital converter for converting the signals held by the sample and hold circuit to digital signals for the microprocessor.

Variable gain means may also be provided to amplify peak signals and bring them to the same value. The variable gain means may then include a programmable read-only memory connected to the microprocessor to be addressed by digital signals representative of peak magnitudes in half cycles, the programmable read-only memory being programmed to read out scale factors determined by applied addresses. The variable gain means may then also include a multiplying digital-to-analogue converter which is connected to receive digital sample signals representative of apparatus input signals at one input and to receive the signals read out from the programmed read-only memory at another input.

If a companding analogue to digital converter is used, the processing means may

operate on signals from the converter by the addition of a constant number representative of the desired maximum output level of the apparatus and the subtraction of a number representative of the measured peak signals to provide signals representative of the logarithm of the required apparatus output signals, a companding digital-to-analogue converter being provided to generate apparatus output signals.

Radio transmitters, or receivers, or telephone channels may include apparatus according to the invention as an aid to intelligibility and efficiency of transmission.

The characteristic value of portions of the output signal may additionally depend on other signals, for example a feedback signal.

According to a second aspect of the present invention there is provided a method of automatic signal level adjustment including the step of measuring the value of a characteristic of each of successive portions of an input signal, the portions being consecutive or separated by intervals, and the characteristic of each portion being related to the magnitude of at least one instantaneous value of the signal in that portion, and the step of operating on each portion of the input signal in accordance with the value measured for that portion only provided the measured value is above a predetermined limiting threshold value, to provide an output signal having successive portions in each of which the same characteristic, or another characteristic related to the magnitude of at least one instantaneous value in that portion, is brought within a predetermined range of values.

The above mentioned examples and preferable ways of putting the invention into effect given for the first apsect of the invention apply also to the second aspect.

The apparatus of the invention may be provided in part or whole by a programmed computer and the method of the invention may be performed by a programmed computer.

Certain embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:—

Figure 1 is a simplified block diagram of apparatus according to the invention;

Figures 2a and 2b show waveforms occurring in the apparatus of Figure 1;

Figure 3 is a more detailed block diagram of apparatus according to Figure 1;

Figure 4 shows a schematic diagram illustrating the operation of part of the apparatus of Figure 3,

Figure 5 shows a flow diagram illustrating a program for the microprocessor of Figure 3,

Figure 6 is a graph of input power level against expected output power level for different noise thresholds for the circuit of Figure 3,

Figure 7 shows expected graphs relating to signal to noise ratio for the circuit of Figure 3,

Figure 8 is a graph of articulation against signal to noise ratio expected for the circuit of Figure 3,

Figure 9 is a block diagram of another apparatus according to Figure 1,

Figure 10 is a schematic of the processes which occur in the microprocessor of Figure 9,

Figure 11 shows a flow diagram illustrating a program for the microprocessor of Figure 9,

Figure 12 shows the input/output characteristic of a companding analogue to digital converter used in Figure 9, and

Figure 13 shows input/output characteristics for the apparatus of Figure 9.

In order to introduce the implementation of the invention it is first explained with reference to the simplified block diagram of Figure 1. Electrical input signals representative for example of speech are applied to a terminal 10 and pass to a circuit 11 which detects each positive and negative peak and applies a control voltage to a gain controlled stage 12. Signals from the terminal 10 also pass by way of a delay circuit 13 so arranged that each half cycle passes through the stage 12 when the control voltage is determined by the peak found in that half cycle. As successive half cycles pass from the delay circuit 13 the control voltage applied to the stage 12 is changed so that it always depends upon the peak measured for the half cycle then applied to the stage 12.

In this way an input signal 14 (see Figure 2) is amplified to have the form shown at 15. The peak detector circuit 11 is constructed to apply a control voltage giving unit gain, or low fixed gain, if the peak detected at any half cycle is less than a noise threshold shown at 16 in Figure 2. In this way only signal is enhanced and not noise. The control voltage applied to the stage 12, when peaks are above the noise threshold, is such that each peak is adjusted to a magnitude which is the maximum which can be handled without distortion by apparatus connected to an output terminal 17. Thus if the input signal is a speech signal from a microphone and the output terminal 17 is connected to a transmitter, the transmitter always receives its input signal at an optimum level and with an improved signal to noise ratio. The control signal developed by the peak detector 11 and applied to the stage 12 is shown at 18 in Figure 2.

One way of implementing the apparatus of Figure 1 will now be described with reference to Figure 3. An input amplifier 20 connected to receive signals from the input terminal 10 provides an appropriate input impedance for the source, for example a microphone, which is connected to the terminal 10. In addition the amplifier 20 has the gain necessary to raise the maximum expected peak input signal to the voltage which fully loads a sample and hold circuit 21 connected at the output of the amplifier. Equalisation to band limit the output spectrum of signals applied to the terminal 10 to less than half the sampling rate of the sample and hold circuit 21 is also achieved by the amplifier 20.

The sample and hold circuit 21 momentarily retains each of a series of instantaneous values of the signal from the amplifier 20 and applies them to an analogue to digital converter (A.D.C.) 22. Sampling is carried out at a rate such that at the highest frequency to be handled one sample occurs in each half cycle.

The analogue to digital converter generates an 8 bit signal for each sample. The first bit indicates the sign of the sample and the remaining 7 bits indicate the magnitude of the sample to the nearest one of 128 levels.

As a result of sampling followed by analogue to digital conversion the 7 bit number specifying the highest positive level is 7 zeroes while the lowest possible positive level is 7 ones. For negative samples the lowest magnitude is specified by 7 zeroes while the most negative is specified by 7 ones. In order to specify the levels in positive half cycles by numbers which increase with increasing magnitude, in the same way that negative half cycles are specified, each magnitude bit of a sample is passed to an exclusive OR gate in a group of such gates, shown as a single gate designated 23. The sign bit for each sample is applied to an inverter 24 the output of which is connected to an input of each EX-OR gate in the group 23. As a result, the 7 magnitude bits applied at an input/output port 25 signify binary numbers which increase from zero to 128 as the magnitude increases in either the positive or negative sense.

In Figure 3 where a numeral is adjacent to an oblique stroke on a line representing connections between circuits, the numeral indicates the number of bits passing by way of the connection. Thus the input/output port 25 receives the 7 magnitude bits of each sample from the group of EX-OR gates 23 and the sign bit from the converter 22.

The input/output port 25 controls signals to and from a microprocessor 26 and it comes under the control of a program stored in the microprocessor.

The 7 magnitude bits and the sign bit pass under the control of the microprocessor program through the input/output port and the microprocessor itself into a memory 27 which is partially illustrated in Figure 4, in that it is notionally divided into two 128 byte random access memory (R.A.M.) sections 30 and 31. The memory however also includes a read only memory (R.O.M.) section of 256 bytes which stores the program for the microprocessor.

Figure 4 shows a path for signals from the A.D.C. 22 to the two R.A.M. sections 30 and 31 but although this path includes the circuits 23 to 26 they are omitted from Figure 4 for simplicity. R.A.M. section 31 stores the 8 bits of each sample in a "first-in first-out" mode under the control of the microprocessor program. Thus after 128 samples have been stored the first sample to be stored appears at the output of the section 31. The microprocessor under the control of the program determines and calculates from the samples the peak value of each half cycle of the input waveform, these peaks also being stored on a first-in first-out basis. The microprocessor under the control of its program also test each sample as it is emitted from the section 31 of the R.A.M. to see, by reference to the sign bit, whether a zero crossing has occurred. As soon as a zero crossing is detected the peak value for the subsequent half cycle is passed from the R.A.M. section 30 to a programmed read-only memory (P.R.O.M.) 32 and a digital to analogue converter (D.A.C.) 33. Again although the peak values from the section 30 of the R.A.M. pass by way of other circuits before reaching the P.R.O.M. 32, for simplicity these circuits are not shown in Figure 4.

When a digital input signal representative of the peak value of a half cycle is used to address the P.R.O.M. the output signal is, by virtue of the programming of the P.R.O.M., a digital signal representing the scaling factor required to bring that peak up to the maximum system level that is the required constant peak amplitude for all half cycles having peaks above the noise threshold. The scaling factor is approximately equal to 128 divided by the applied half cycle peak. Faster machine operation is obtained by using a P.R.O.M. to provide the scaling factor than by using the microprocessor to calculate the scaling factor, although of course, with more powerful microprocessors the same speed can be maintained when the P.R.O.M. is not used, or if a slower operation speed is adequate the P.R.O.M. may be omitted.

The scaling factor obtained is applied to control a multiplying digital to analogue

converter (M.D.A.C.) 34 which again is shown connected directly to the R.A.M. section 31 but in fact is connected by way of several other circuits to the output of the memory 27. The first sample emitted by the R.A.M. section 31 after a zero crossing is detected, is applied by the microprocessor 26 to the M.D.A.C. 34 as soon as the scaling factor appropriate to the half cycle containing that first sample has been applied thereto. Hence every half cycle of analogue signal from the output of the M.D.A.C. 34 has the same peak value, provided the corresponding input half cycle at the terminal 10 has a peak which was greater than the noise threshold.

The program for the microprocessor 26 is based on the flow diagram shown in Figure 5. Firstly a sample is passed from the head of a first queue (Q_0) formed in the R.A.M. section 31 to the M.D.A.C. 34 in an operation 35. The next input sample is then added at the tail of the first queue in an operation 36. Next a test 37 is carried out on the next sample to be added to the tail of the first queue to determine whether the sign of this bit is different from that of the last sample added to the first queue. If no change in sign has occurred a further test 38 is carried out to determine whether the sample just passed to the first queue is greater in amplitude than the previous sample. If not the microprocessor rests for two intervals 40 and 41 before recommencing the flow cycle at the first operation 35 by way of a jump-to-start 45. If on the other hand the new sample is greater than the previous sample the new sample is temporarily held by the microprocessor overwriting any previous temporary sample in an operation 42 and then after an interval 41 the flow cycle is repeated commencing with the operation 35.

If the result of the test 37 indicates that a zero crossing has occurred at the tail of the first queue, then the value held as a result of the test 42 is stored in the R.A.M. section 30 as part of a second queue (Q_1) in an operation 42. A test 43 is then carried out to determine whether a sign change has occurred at the output of the first queue. If not the cycle starts again at operation 35 after an interval 44 and the jump to start 45. If, on the other hand, a sign change has occurred at the head of the first queue then an operation 46 transfers the digital signal at the head of the second queue to address the P.R.O.M. 32.

The second queue is so controlled by the microprocessor program that although the R.A.M. section 30 may not be full, the sample at the head of the second queue is always ready to be passed to P.R.O.M. 32. Alternatively, the program may pack the R.A.M. section 30, for example by repeating peak values, so that it is always full and the required peak value is available at the head of the second queue when the samples from the corresponding half cycle start to be emitted from the head of the first queue.

Returning now to Figure 3 to follow the passage of samples and peaks from the microprocessor in more detail, digital signals indicating the mangitude of half waveform peaks are passed to a comparator 48 under the control of the microprocessor program by way of the microprocessor 26 and the input/output port 25. Peak values for half waveforms are compared with a noise threshold in the comparator 48. The threshold is set up by means of seven switches in a group of switches shown as a single switch 50. Each switch is closed applying a voltage representing a "one" to the comparator 48 if the digital signal representing the threshold is to have a "one" in a bit position represented by that switch. If a peak signal is greater than the threshold an enabling signal is passed by way of a switch 51 to an each gate in a group of AND gates shown as a single gate 52. Should it be required to pass the signal through the system without automatic gain control the switch 51 may be switched to the position in which the gates in the group 52 do not receive the enabling signal.

The seven magnitude bits of each peak signal are also passed to the AND gates in the group of gates 52 so that the P.R.O.M. 32 is only addressed when a peak signal is above the noise threshold.

Since the P.R.O.M. has only a 7 bit output the values of 128 divided by the various peak values which are stored in the P.R.O.M. and passed to the D.A.C. 33 are approximate. They are chosen to provide half cycles with constant peaks at the output of the M.D.A.C. 34 as nearly as this is possible.

Magnitude bits of samples from the first queue in the R.A.M. section 31 of the memory 27 are passed under the control of the microprocessor program by way of the microprocessor 26 and the input/output port 25 to a group of exclusive OR gates shown as a single EX OR gate 54. Each sign bit passes by the same route to an inverter 53 and thence to each gate in the group 54. The inverter 53 and the gates in the group 54 reverse the process carried out by the gates 23 and the inverter 24 before the sample signals are passed to the M.D.A.C. 34. The sign bit also passes directly to the M.D.A.C. 34 from the input/output port 25.

A low pass filter 55 attenuates the sampling steps in the output waveform from the M.D.A.C. so smoothing the waveform generated, and an output amplifier 56

provides appropriate matching and a suitable output level for subsequent circuits.

The component circuits used in Figure 3 may, for example, be as follows:—

Processor 26:
Intel 8080A Microprocessor chip
Intel 8224 Clock generator
Intel 8228 System controller
Input/output port 25: Intel 8225A.
Memory 27:
Random access memory-2 off Intel P 2101A.
Read only memory-2 off Intel D 3601.
Analogue-to-digital converter 22: Burr Brown ADC 82 AG.
Sample-and-hold circuit 21: Burr Brown SHC 80 KP.
Digital-to-analogue converter 33: Hybrid Systems Corporation DAC 334—8
Multiplying digital-to-analogue converter 34: Hybrid Systems Corporation DAC 331—8.

With the circuit described in connection with Figure 3 using a type 8080A microprocessor, one cycle of the program takes approximately 166μ seconds. The microprocessor provides control signals by way of channels 57 and 58 to control the sampling rate of the circuit 21 and the conversion carried out by the A.D.C. 22. Thus the sampling rate is approximately 6 KHz, and therefore the bandwidth of the apparatus is 3 KHz.

The first queue in the R.A.M. section 31 holds 128 samples and each sample therefore takes 166μ secs.$\times$128=21.2 milliseconds to pass from tail to head of this queue. Therefore the signal delay is 21.2 milliseconds which is thought to be sufficiently small as to be unnoticeable to an operator when speaking into a microphone and at the same time hearing the processed signal.

With 128 samples in the first queue, the lowest frequency that the apparatus can handle is

$$\frac{10^3}{21.2\times 2}=20\text{Hz}$$

The frequency range of the apparatus is therefore 20 Hz to 3 KHz.

Clearly the bandwidth and signal delay can be varied by changing the number of samples in the first queue or by writing a processor program having a different cycle time.

The effect of changing the noise threshold on a system using a type 8080A microprocessor and of the form shown in Figure 3 is expected to be as shown in Figure 6 which is power level input/output charateristic. Curves are shown for various values of the noise threshold, designated T, and the values shown for T are the percentages of the maximum system level at which the noise threshold is set. Hence when T=0 there is no noise threshold and the output level is independent of input variation over a range of 35 dBm. Even signals at a level of −50 dBm may be increased to a satisfactory listening level.

At the other extreme when T=100% no peak amplitude level adjustment is carried out and the characteristic is linear.

The characteristic shown in Figure 6 was obtaining with linear encoding and decoding carried out by the A.D.C. 22 and the M.D.A.C. 34 but linear encoding has the disadvantage that small signals are encoded in magnitude increments which are relatively coarse, while large signals are encoded using relatively small increments. An improvement can be obtained by using a companded characteristic, where near zero, encoding increments are small while for large signals they are corresponding large. With a companded encoder, the level control shown in Figure 6 may be extended from −50 dBm to about +7 dBm.

Figure 7 shows the expected signal to noise ratio improvement for the system of Figure 3 using the 8080A microprocessor. Three curves are shown:—

Curve 57 relates to equal input and output signal to noise ratios,

Curve 58 shows the signal to noise ratio improvement which, as can be seen, reaches a maximum at an input signal to noise ratio of about 6 dB, and

Curve 59 shows a normalised output signal to noise ratio of

$$\frac{S+N}{N}$$

Values for calculating the improved signal to noise ratio are measured by transmitting noise below the noise threshold with a gain of unity when noise level is to be measured, and when signal level is to be measured transmitting speech above the threshold which is elevated to the system maximum level.

Another indication of performance of the system of Figure 3 which is expected to be obtained with the above mentioned microprocessor is shown in Figure 8. Here articulation, that is percentage of words recognised by a group of male and female listeners, is plotted against signal to noise ratio. The three dashed curves 61, 62 and 63 show unprocessed speech and correspond to the loudest talker, medium talker and quitest talker, respectively. The solid curve 64 represents speech processed by the apparatus of Figure 3 for all types of talkers. It will be seen that for the medium and

quitest talkers the articulation is greatly improved so that unintelligible speech may be made intelligible. The inclusion of the processor at the input to a noisy voice channel is worthwhile if the channel signal to noise ratio is worse than 28 dB. Most multichannel systems have a signal to noise ratio which is less than this. It will be appreciated that many changes can be made in the apparatus of Figure 3. For example the microprocessor 26 may be chosen so that it can handle a larger number of bits indicating sample size. The microprocessor may also take over some of the functions of other parts of the circuit, for example it could make the conversions carried out by the exclusive OR gates 23 and 54 and their associated inverters 24 and 53. The microprocessor may also carry out the multiplication carried out by the P.R.O.M. 32 and the M.D.A.C. 34 and the comparison carried out by the comparator 48. In fact apart from analogue to digital conversion and digital to analogue conversion, the whole process of peak amplitude level control can be carried out by a full size or micro computer. Equally all or part of the microprocessor could be replaced by dedicated hardware.

Since the multiplication by two of a binary number can be achieved by the addition of zeroes to the least significant end of the number, the P.R.O.M. 32 and the M.D.A.C. 34 may be replaced by a sub-routine added to the microprocessor program. The sub-routine tests each halfwave peak value against the maximum output level of the system and if the half cycle peak is greater than half the maximum system output level no change is made; if it is between half and a quarter of the system level all samples in that half cycle are doubled by adding one zero; and if it is between zero and a quarter of the maximum system level all samples in that half cycle are quadrupled by the addition of two zeroes. Clearly other schemes of a similar nature may be employed.

The noise threshold reference applied to the comparator 48 may be variable to suit different signal to noise ratios and means may be provided for measuring the signal to noise ratio and generating a noise threshold reference in accordance with the ratio measured.

A disadvantage in the operation of the apparatus of Figure 3 is that when, for example, half cycle peaks in speech span the noise threshold 16 of Figure 2a portions of the same word may be comparatively quiet when reproduced while others are amplified fully. This effect can in some circumstances make speech difficult to understand.

One method of overcoming this disadvantage is to use a limiting threshold 66 (see Figure 2a) so that any half cycles having peaks falling below this threshold are amplified by a fixed gain greater than unity, for example

$$\frac{S_{max}}{T_L}$$

where S_{max} is the maximum required output level which the apparatus is to supply and T_L is the threshold level 66.

In an alternative unity gain is employed for half cycles with peaks below the noise threshold 16, a fixed gain is employed for signals between the noise threshold 16 and the limiting threshold 66 but above the limiting threshold gain is variable and depends on the peak value of the half cycle.

As far as the variable gain employed between the two thresholds is concerned this may be equal to either

$$\frac{S_{max}}{T_L}$$

or

$$\frac{S_{max}}{T_L - T_N}$$

where T_N is the noise threshold level. With a gain of

$$\frac{S_{max}}{T_N}$$

a low value for T_L will accommodate a wider range of variation in level at the input whilst maintaining a constant output but it will accentuate background noise during periods when speech is absent and it is therefore preferable to incorporate the noise threshold (T_N)

The apparatus of Figure 9 follows the same basic pattern as is outlined with reference to Figure 1 and follows the scheme outlined in the previous paragraph. Input signals from an input terminal 10 pass to an amplifier and bandpass filter 67 which has the gain necessary to raise the maximum expected peak input signal to the voltage which fully loads a sample and hold circuit 68. Instantaneous values of the input signal are held by the sample and hold circuit 68 until passed to a companding analogue to digital converter (ADC) 69 under the control of a "sample command" signal from the ADC.

The ADC generates an 8 bit signal for each sample. The first bit indicates the sign of the sample and the remaining 7 bits indicate the magnitude of the sample to the

nearest one of 128 levels arranged on a logarithmic scale so that in effect the output samples from the ADC are the logarithm of the signal applied thereto.

As in Figure 3 where a numeral is adjacent to an oblique stroke on a line representing connections between circuits, the numeral indicates the number of bits passing by way of the connection.

The operations of detecting half cycle peaks and applying appropriate feed forward gain are carried out by a microprocessor 71 having an input/output port 72 controlled thereby.

The seven magnitude bits and the sign bit pass under the control of the microprocessor program through the input/output port and the microprocessor itself to a memory 73 which is notionally divided into two 256 bit R.A.M. sections. The memory also includes an R.O.M. section of 256 bits which as with Figure 3 store, among other data, the program for the microprocessor.

The processes which take place in the microprocessor will now be briefly described with reference to Figure 10. Signals from the companding ADC 69 are formed into a samples queue Q1, zero crossings are detected in a process 74, and current peak values (CPVs) are detected by comparison with earlier peak values in a half cycle and also compared with the threshold values in a process 75.

When a zero crossing is detected by the process 74, the CPV, or one of the values T_L or T_L-T_N, or S_{max} if the CPV is between the thresholds or lower than the threshold 16, respectively, is added to a peaks queue Q2.

A further process of zero crossing detection 76 is carried out at the head of the queue Q1 and when a zero crossing is detected, the peak value at the head of the queue Q2 is read out and applied to an output scaling operation 77. In this operation the sample peak value S_p is taken from $S_{max}+S_I$, where S_I is the current sample value. Since by virtue of the companding ADC, S_p and S_I are in logarithmic form and furthermore S_{max} is also a logarithmic value, the output of the process 77 is the logarithm of

$$\left(\frac{S_{max}}{S_p}\right) S_I.$$

Since the peaks queue Q2 does not only contain true peak value S_p but also by substitution S_{max} if the half cycle peak was below the noise threshold 16; or either T_L or T_I or (T_L-T_N) where a half cycle peak fell between the thresholds, the operation 77 in effect amplifies by the appropriate one of the three factors mentioned.

Signals from the microprocessor 71 pass by way of the input/output port 72 to a companding digital to analogue converter (DAC) 78 which has the inverse characteristic of the ADC 69 and so converts its digital logarithmic input to a linear analogue output. Signals from the DAC 78 are passed to a low pass filter and output amplifier 79 which serves the same function as the filter 55 and amplifier 56 of Figure 3.

In Figure 9 a reference digital signal representative of the noise threshold is passed by way of switch means 81 to the input/output port 72 and a signal representative of the limiting threshold passes by way of switch means 82 to the input/output port.

A flow chart for the program of the microprocessor 71 is shown in Figure 11. Description of the flow chart is started at process 83 with the beginning of a new half cycle, where the first input sample is loaded as the CPV there being no other suitable sample available. A test 84 is then carried out to determine whether a zero crossing has occurred at the output of the queue Q1. If so a new peak value is applied to the scale process 77 (see Figure 10) in operation 85. If not and also after operation 85 the current sample from the output of the queue Q1 is scaled in an operation 86 (equivalent to 77 on Figure 10) and sent to the companding DAC 78.

The next sample is then obtained from the output of the ADC 69 in an operation 87 and placed in the queue Q1. This sample is tested at 88 to discover whether a zero crossing has occurred at the tail of the queue Q1 and if not the current sample is tested at 89 to find out whether it is larger than the previous sample. If not operations 84 to 86 are carried out. On the other hand if the current sample is greater than the previous sample then, in operation 91, the current sample is loaded as the CPV and then the operations 84 to 86 are carried out.

If the result of test 88 is that a zero crossing has occurred then a further test 92 is carried out to see whether the CPV is greater than the limiting threshold 66. If it is then the current CPV is put into the queue Q2 as a peak value for a half cycle. However if the CPV is smaller than the threshold level 66 a further test 94 is carried out to find out whether the CPV is greater than the noise threshold 16. If so then the CPV is replaced with S_{max} in an operation 95 and then operation 93 is carried out so that in fact instead of putting a CPV into the queue Q2 the value S_{max} is put into the queue where it can be regarded as a modified CPV.

If in operation 94 the CPV is found to be greater than the noise threshold 16 then the value (T_L-T_N) is used to replace the CPV in operation 96. Thus again for operation 93

the CPV added to the queue Q2, that is $(T_L - T_N)$ can be regarded as a modified CPV value. If the gain to be used between the threshold levels is to be dependent on T_L instead of $(T_L - T_N)$, then in operation 96 the CPV is replaced with T_L.

The following components may be used in Figure 9, for example:—

Microprocessor 24: MOSTEK Z80.

Input/output port 72: MOSTEK Z80, PIO

Memory 73:

(random access memory)-Intel P 2111

(read only memory)-Intel 8708.

Companding analogue to digital converter 69: Precision Monolithics Inc. DAC—76.

Sample and hold circuit 21: DATEL SHM—LM—1

Companding digital to analogue converter 78: Precision Monolithics Inc. DAC—76.

Figure 12 shows the input/output characteristic for normalised inputs and outputs of the analogue to digital converter which follows the "Bell μ-255 law; that is

$$y = \frac{\ln(1+\mu x)}{\ln(1+\mu)}$$

where y is the normalised digital output value,

x is the normalised analogue input value,

ln signifies Naperian logarithm, and

μ=255.

When a noise threshold is used the input/output characteristic for the apparatus of Figure 9 is as shown in Figure 13. The characteristics shown are for an input signal having a Gaussian distribution. Each curve corresponds to a chord of Figure 12 and is designated by the same number as that chord. For example if the threshold level 66 is set to Odb then the input/output characteristic is the line 7, that is gain in constant at unity.

In a further example, the limiting threshold level 66 is fixed at 31.3db and line 2 is the characteristic obtained so that there are three areas of operation:— one below the noise threshold where substantially unity gain is employed, one between the noise threshold and −31.3db where the gain is fixed and one above −31.3db where the gain varies in accordance with the peak level in a half cycle.

While a number of specific embodiments of the invention have been described it will be appreciated that the invention can be put into practice in many other ways.

WHAT WE CLAIM IS:—

1. Apparatus for automatic signal level adjustment, including processing means for measuring the value of a characteristic of each of successive portions of an input signal, the portions being consecutive or separated by intervals, and the characteristic of each portion being related to the magnitude of at least one instantaneous value of the signal in that portion, and the processing means also being arranged to operate on each portion of the input signal, in accordance with the value measured for that portion only provided the measured value is above a predetermined limiting threshold value, to provide an output signal having successive portions in each of which the same characteristic, or another characteristic related to the magnitude of at least one instantaneous value in that portion, is brought within a predetermined range of values.

2. A method of automatic signal level adjustment including the step of measuring the value of a characteristic of each of successive portions of an input signal, the portions being consecutive or separated by intervals, and the characteristic of each portion being related to the magnitude of at least one instantaneous value of the signal in that portion, and the step of operating on each portion of the input signal, in accordance with the value measured for that portion only provided the measured value is above a predetermined limiting threshold value, to provide an output signal having successive portions in each of which the same characteristic, or another characteristic related to the magnitude of at least one instantaneous value in that portion, is brought within a predetermined range of values.

3. Apparatus or method according to Claim 1 or 2 wherein the portions are consecutive, and each portion is a half cycle, or a group of less than ten half cycles of the input signal.

4. Apparatus or method according to Claim 1, 2 or 3 wherein the said characteristic of the input signal and/or the output signal is one of the following:— peak magnitude of the portion, a root or the mean or the root mean square of the said peak magnitude, or the median magnitude of the instantaneous values of the portion.

5. Apparatus according to Claim 1, 3 or 4 wherein the processing means is arranged to generate a control signal which varies in accordance with measured values of the characteristic of the portions of the input signal, and to amplify or attenuate the portions of the input signal in accordance with corresponding portions of the control signal.

6. Apparatus according to Claim 1 or any of Claim 3 to 5, wherein the characteristic of the portions of the input and output signals is peak magnitude of each half cycle

of the input and output signals, and the processing means is arranged to compare each input-signal half-cycle peak magnitude with the predetermined limiting threshold value, and to amplify a half cycle by a variable gain only when the peak magnitude thereof is above the limiting threshold value to bring all the half cycles of the output signal, corresponding to those input half cycles so amplified, to substantially the same value.

7. Apparatus according to Claim 6 wherein the processing means is arranged to compare each input-signal half-cycle peak magnitude with a noise threshold value in addition to and below the limiting threshold value, and amplify each half cycle either by a comparatively low gain or unity gain if the peak value thereof is below the noise threshold, or by a comparatively high gain if the peak value thereof is between the limiting threshold and the noise threshold, or by a variable gain related to the peak value of that half cycle if the peak value is above the limiting value.

8. Apparatus according to Claim 7 wherein the comparatively high gain is equal to the maximum desired output signal level divided either by the limiting threshold value or by the limiting threshold value minus the noise threshold value.

9. Apparatus according to Claim 6 wherein the processing means is arranged to amplify each half cycle having a peak value below the limiting threshold value by a gain equal to the maximum desired output level divided by the limiting threshold value.

10. Apparatus according to Claim 1 or any of Claims 3 to 9 wherein the processing means comprises a programmed microprocessor and an associated memory.

11. Apparatus according to Claim 10 wherein the processing means also comprises a sample-and-hold circuit for sampling analogue signals and an analogue-to-digital converter for converting the signals held by the sample-and-hold circuit to digital signals for the microprocessor.

12. Apparatus according to Claim 11 wherein the microprocessor is programmed to detect peak values of half cycles, to store first signals representative of samples of apparatus input signals, to store second signals representative of peak values or determined thereby, and to make the first signals for each half cycle of the apparatus input signals available successively at the microprocessor output or internally, and to make available while the first signals are made available the second signal for that half cycle.

13. Apparatus according to Claim 12 wherein the processing means also includes variable-gain means for amplifying the sample signals, and the variable-gain means comprises a programmable read-only memory connected to the microprocessor to be addressed by second signals, the programmable read-only memory being programmed to read out scale factors determined by applied addresses, and a multiplying digital-to-analogue converter connected to receive the first signals at one input and signals read out from the programmable read only memory at another input.

14. Apparatus according to Claim 12, insofar as dependent on Claim 6, wherein the analogue-to-digital converter is a companding converter constructed to provide digital output signals which substantially represent the logarithms of applied input signals.

15. Apparatus according to Claim 14 wherein the microprocessor is programmed to store, when a peak value of a half cycle is between the limiting threshold and the noise threshold, a second signal which is representative of either the logarithm of the limiting threshold value or the logarithm of the difference between limiting threshold value and the noise threshold value, and is programmed when a peak value of a half cycle peak is below the noise threshold, to store a second signal which is representative of the logarithm of maximum desired output signal of the apparatus.

16. Apparatus according to Claim 15 wherein the microprocessor is programmed to add each of the first signals for each half cycle to a signal representative of the logarithm of the maximum desired output signal of the apparatus minus the second signal for that half cycle.

17. Apparatus according to Claim 1 or Claim 3, 4 or 5 for speech input signals, wherein the processing means is arranged to measure pitch period and to detect unvoiced sounds, and to measure the said characteristic over a pitch period when voiced sounds occur in the apparatus input signal and to measure the said characteristic over a fixed interval when unvoiced sounds occur.

18. Apparatus according to Claim 1 or any of Claim 3 to 8 wherein the processing means comprises a computer.

19. Apparatus for automatic signal level adjustment substantially as hereinbefore described with reference to, and as shown in, Figure 3, or Figures 3 and 4 of the accompanying drawings.

20. Apparatus for automatic signal level adjustment substantially as hereinbefore described with reference to Figures 3, 4 and 5 and as shown in Figures 3 and 4 of the accompanying drawings.

21. Apparatus for automatic signal level adjustment substantially as hereinbefore

described with reference to, and as shown in, Figure 9 of the accompanying drawings.

22. Apparatus for automatic signal level adjustment substantially as hereinbefore described with reference to Figures 9, 10 and 11, and as shown in Figure 9 of the accompanying drawings.

23. A method of automatic signal level adjustment substantially as hereinbefore described.

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Chartered Patent Agent,
Agents for the Applicants.

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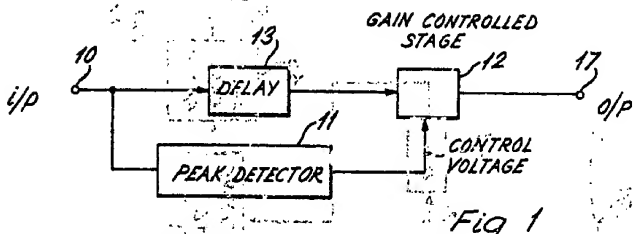

Fig 1

Fig. 2a

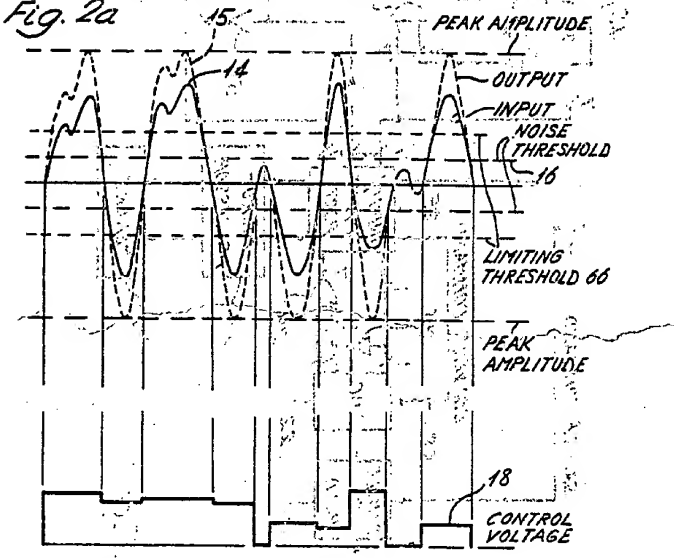

Fig. 2b

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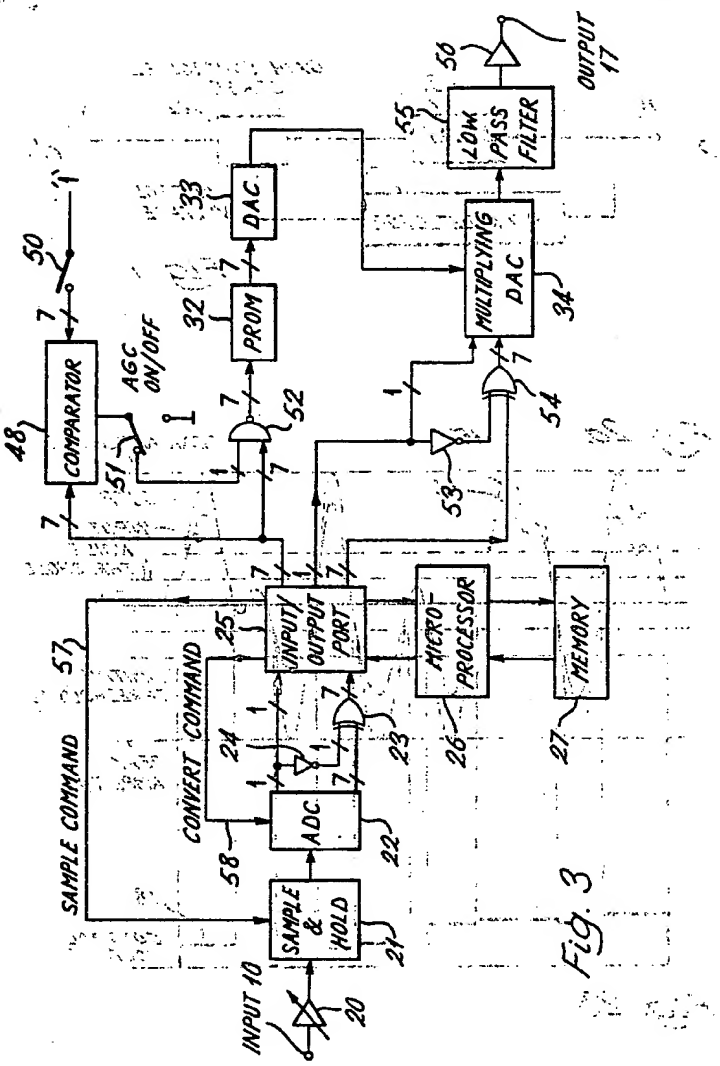

Fig. 3

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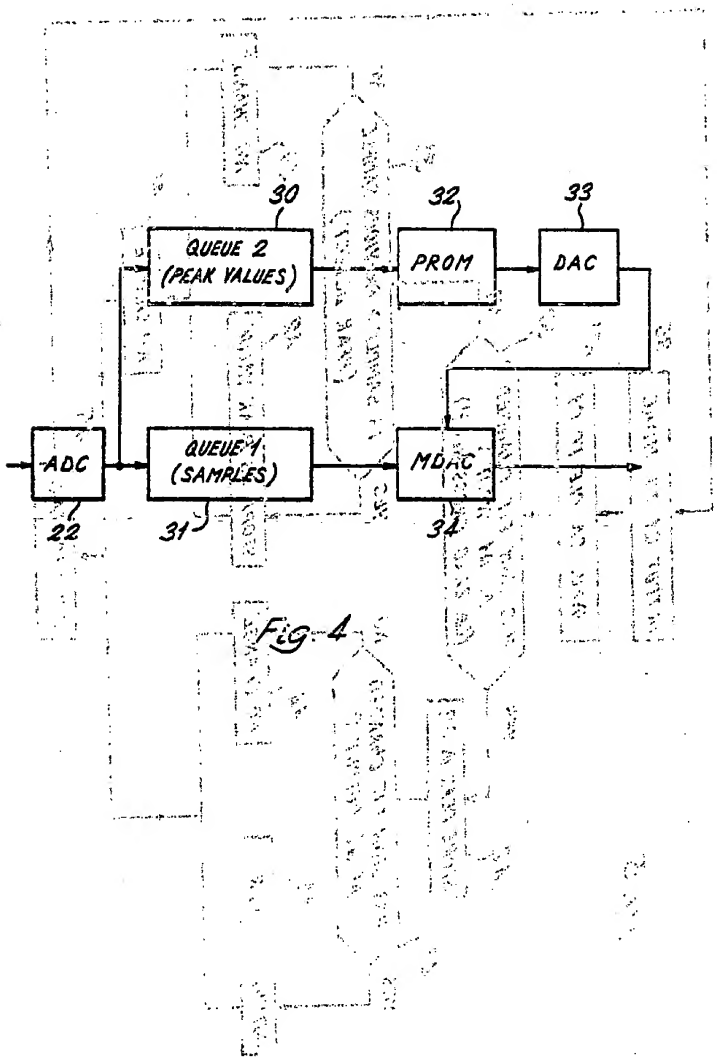

Fig. 4

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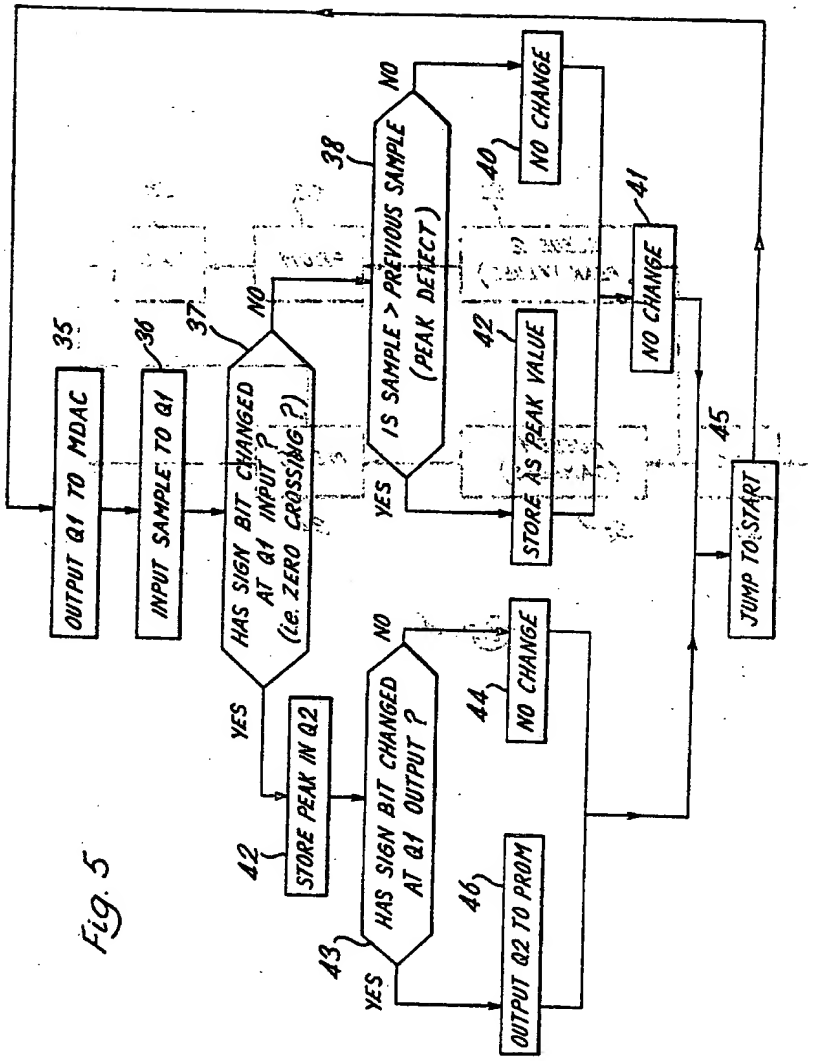

Fig. 5

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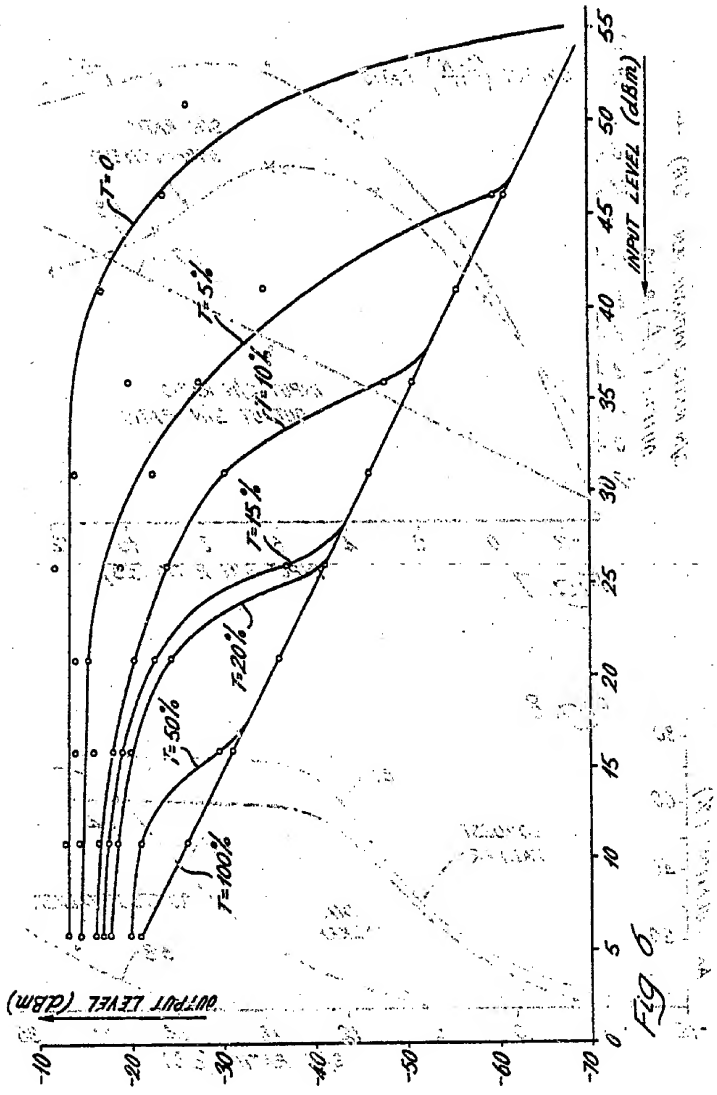


Fig 6

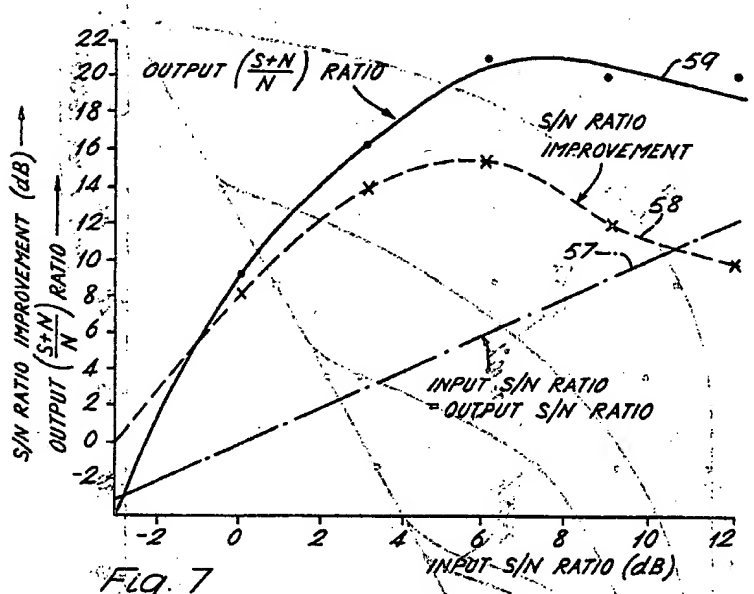
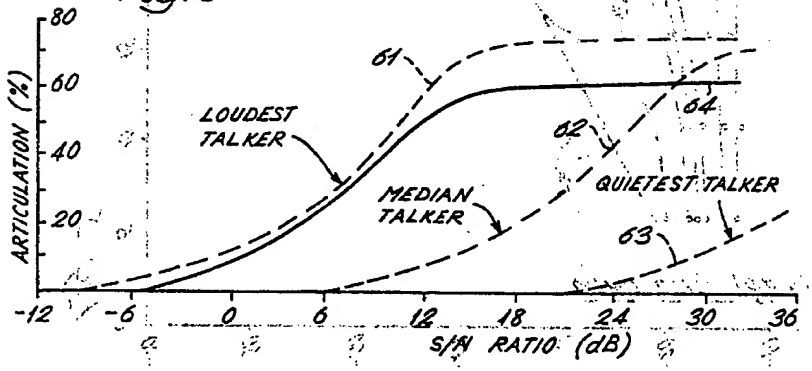

OUTPUT (S+N/N) RATIO
59
S/N RATIO IMPROVEMENT
58
57
INPUT S/N RATIO = OUTPUT S/N RATIO
S/N RATIO IMPROVEMENT (dB) — OUTPUT (S+N/N) RATIO —
INPUT S/N RATIO (dB)

Fig. 7

Fig. 8


61
LOUDEST TALKER
62
64
MEDIAN TALKER
QUIETEST TALKER
63
ARTICULATION (%)
S/N RATIO (dB)

1599401 COMPLETE SPECIFICATION
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Sheet 7

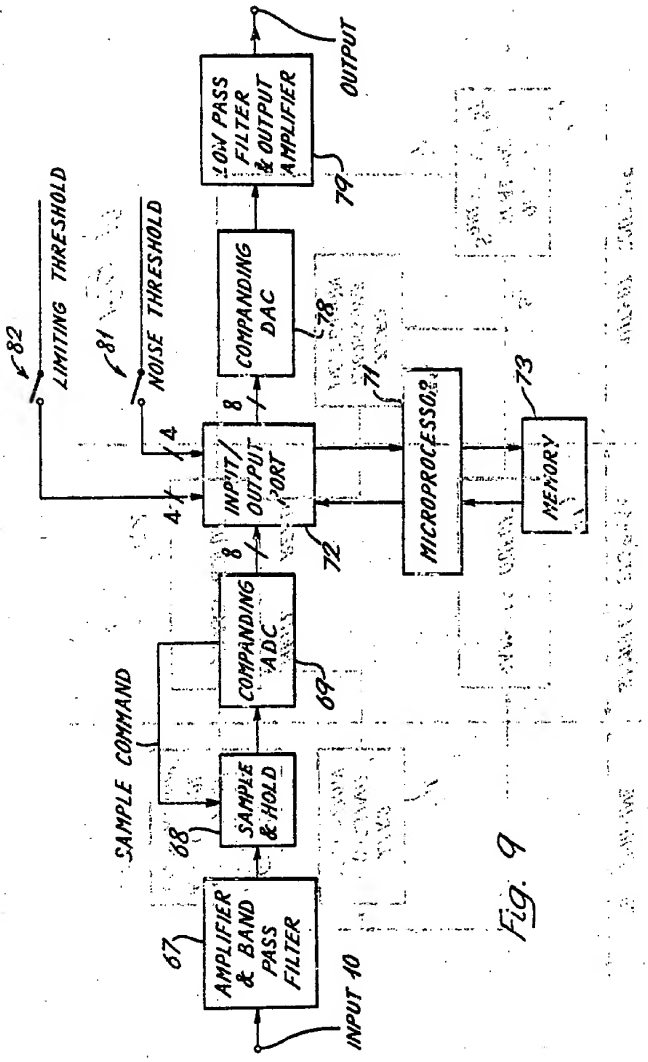

Fig. 9

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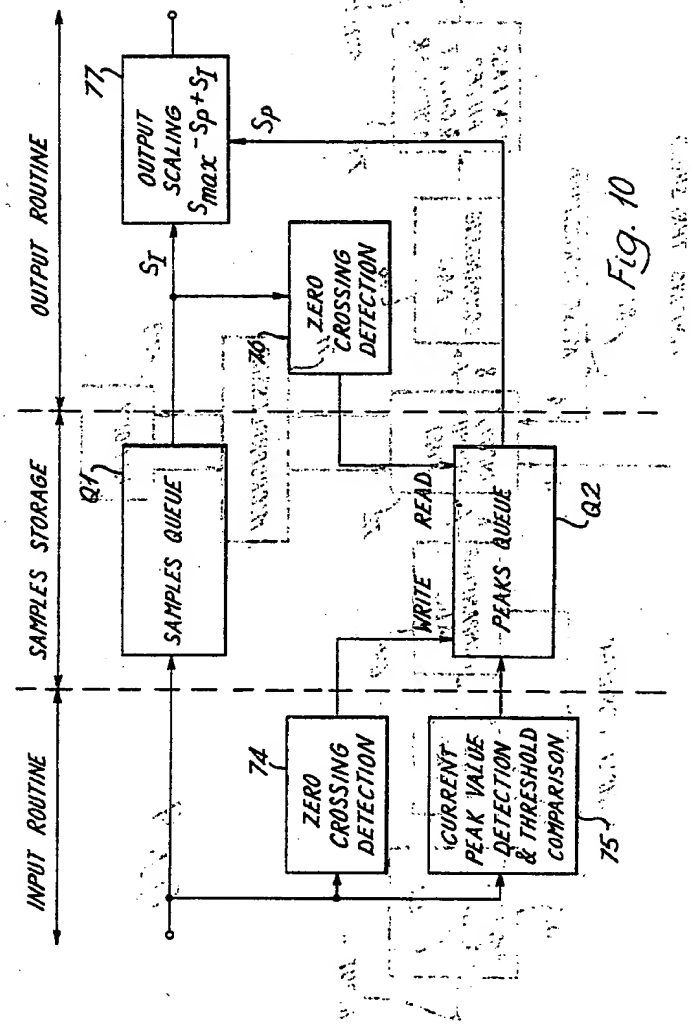
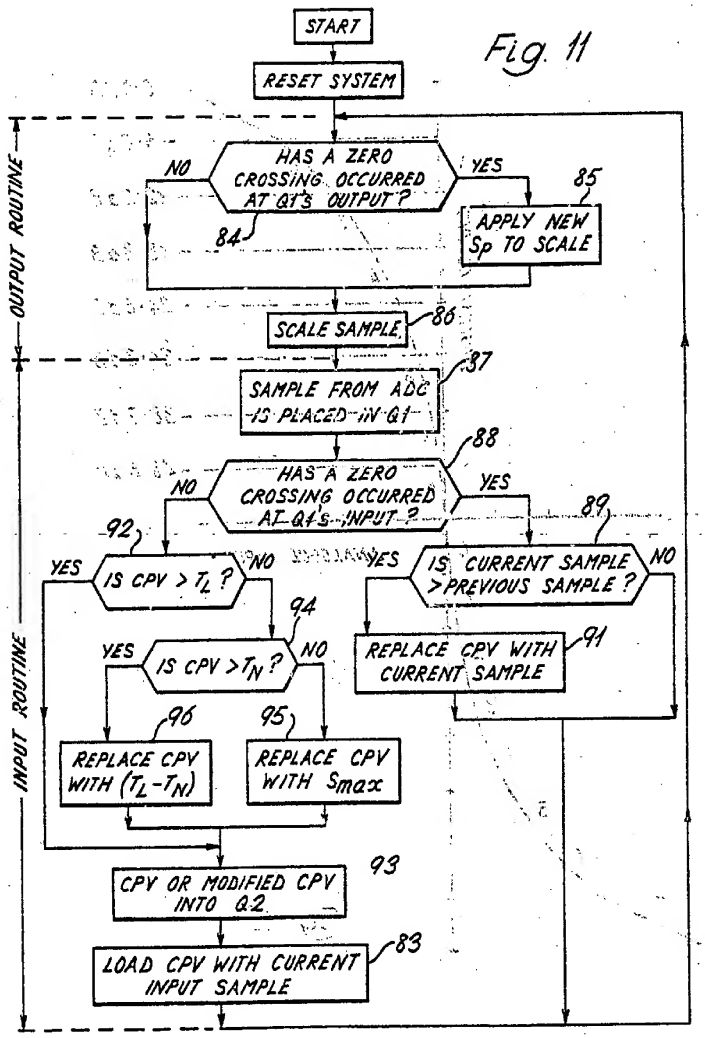


Fig. 10

Fig. 11


START
RESET SYSTEM
OUTPUT ROUTINE
HAS A ZERO CROSSING OCCURRED AT Q1'S OUTPUT ?
NO
YES
84
85
APPLY NEW Sp TO SCALE
SCALE SAMPLE
86
SAMPLE FROM ADC IS PLACED IN Q1
87
HAS A ZERO CROSSING OCCURRED AT Q1'S INPUT ?
88
NO
YES
89
IS CURRENT SAMPLE > PREVIOUS SAMPLE ?
YES
NO
REPLACE CPV WITH CURRENT SAMPLE
91
92
IS CPV > T_L ?
YES
NO
94
IS CPV > T_N ?
YES
NO
96
REPLACE CPV WITH (T_L - T_N)
95
REPLACE CPV WITH Smax
INPUT ROUTINE
93
CPV OR MODIFIED CPV INTO Q2
83
LOAD CPV WITH CURRENT INPUT SAMPLE

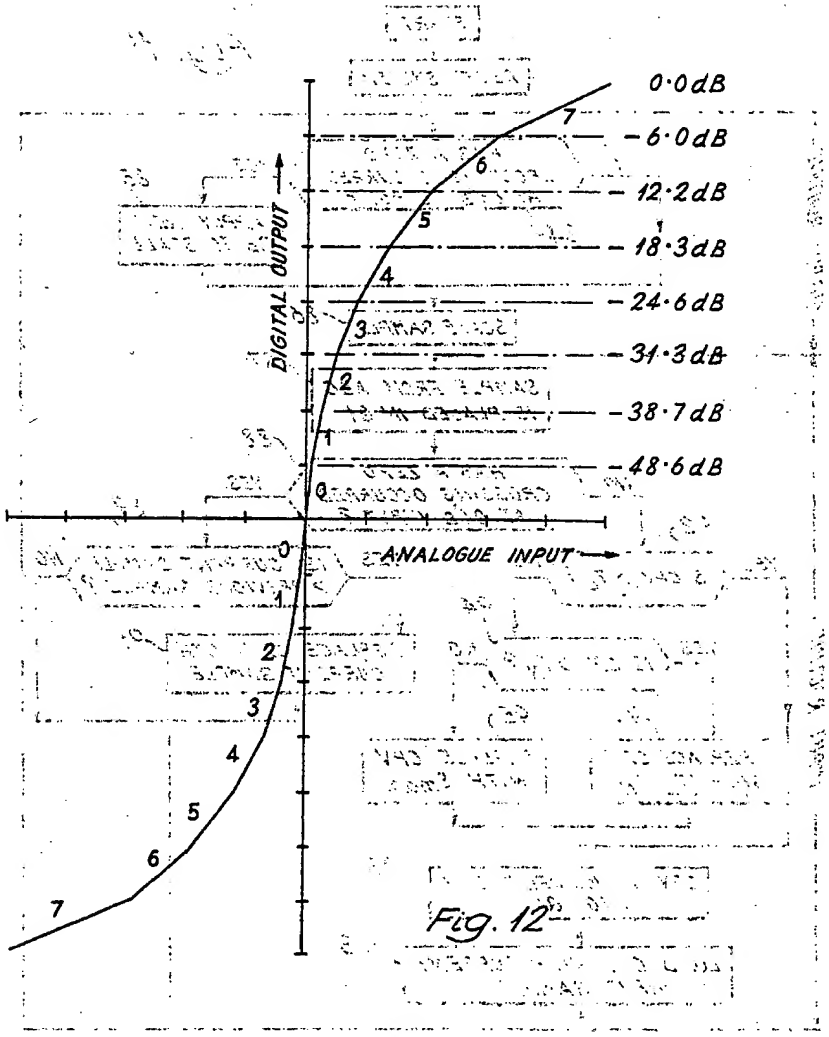

0·0dB
-6·0dB
-12·2dB
-18·3dB
-24·6dB
-31·3dB
-38·7dB
-48·6dB
DIGITAL OUTPUT
ANALOGUE INPUT
0
1
2
3
4
5
6
7

Fig. 12

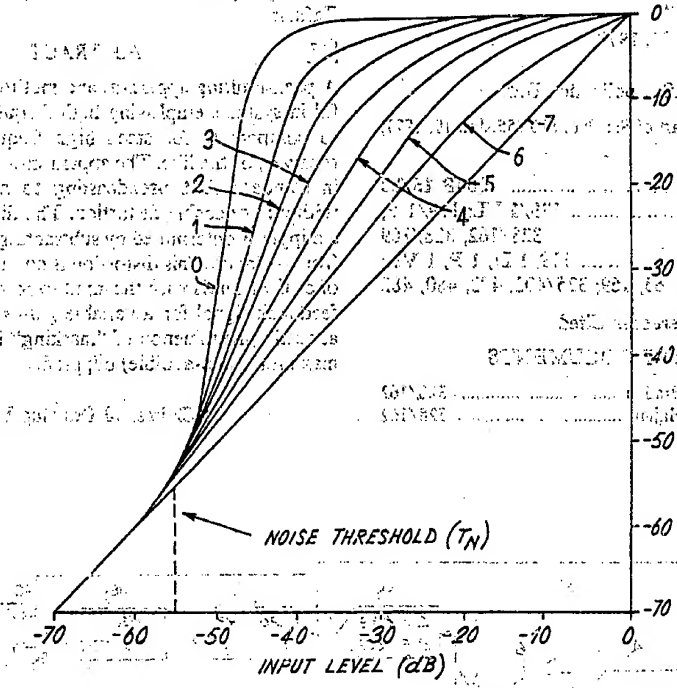

0
-10
-20
-30
-40
-50
-60
-70
OUTPUT LEVEL (dB)
-70
-60
-50
-40
-30
-20
-10
0
INPUT LEVEL (dB)
NOISE THRESHOLD (T_N)
0
1
2
3
4
5
6
7

Fig. 13